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VLSI Design MCQ

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Q1. VLSI is an acronym for _____

- A. Varying large Scale Integration
- B. Varying large Scale Integrity
- **C. Very large Scale Integration**
- D. None of the above

Q2. MOSFETs possess _____

- A. Poor packing density
- **B. Low packing density**
- C. High packing density
- D. None of the above

Q3. _____ to form integrated circuit VLSI technology uses.

- A. diodes
- B. buffers
- C. switches
- **D. transistors**

Q4. What is medium scale integration?

- A. Ten logic gates
- B. Fifty logic gates
- **C. Hundred logic gates**

- **D.** Thousands of logic gates

Q5. Logic design of VLSI is used_____

- A. LIFO
- **B. FIFO**
- C. LILO
- D. FILO

Q6. Which type of MOSFET exhibits no current at zero gate voltage?

- A. Depletion MOSFET
- **B. Enhancement MOSFET**
- C. Both A & B
- D. None of the above

Q7. MOS transistor structure is _____

- **A. symmetrical**
- B. semi symmetrical
- C. non symmetrical
- D. pseudo symmetrical

Q8. The VLSI design flow starts with:

- A. RTL synthesis
- B. Library mapping
- **C. Product specifications**
- D. None of the above

Q9. Which color is used for polysilicon in stick diagram?

- **A. red**
- B. white
- C. brown
- D. orange

Q10. What is the expansion of VLSI

- A. Very Long Scale IC
- B. Very Large Scale IC
- C. Very Long Scale Integration
- **D. Very Large Scale Integration**

Q11. Which model is used for scaling?

- **A. constant electric and voltage scaling**
- B. constant current model
- C. constant voltage scaling
- D. constant electric scaling

Q12. Which is the high level representation of VLSI design?

- A. Logic design
- B. Functional design
- C. HDL program
- **D. Problem statement**

Q13. Gate minimization technique is used to simplify the logic.

- **A. True**
- B. False

Q14. _____ is used to deal with effect of variation.

- A. Chip level technique
- B. Logic level technique
- C. Switch level technique
- **D. System level technique**

Q15. An Antifuse programming technology is predominantly associated with _____

- A. SPLDs
- **B. FPGAs**

- C. CPLDs
- D. All of above

Q16. Which among the following is/are regarded as an/the active resistor/s?

- **A. MOS diode**
- B. MOS switch
- C. MOS transistor
- D. All of above

Q17. Which among the following is/are not suitable for in-system programming?

- A. Flash
- **B. EPROM**
- C. EEPROM
- D. All of above

Q18. In floorplanning, placement and routing are _____

- A. Front end
- **B. Back end**
- C. Both A & B
- D. None of the above

Q19. The difference between V_{OH} and V_{IH} voltages is known as

- A. input margin.
- **B. noise margin.**
- C. output differential.
- D. input level.

Q20. The abbreviated designation for input current with a HIGH input is

- **A. I_{IH}**
- B. I_{IL}
- C. V_{IH}
- D. I_{OL}